DEVKIT-MPC5744P

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Revision Information

Rev	Date	Designer	Comments
X1	6 July 2016	Jun Qiao	Initial
X2	12 July 2016	Jun Qiao	Update MCU decoupling, add boot section
X3	19 July 2016	Jun Qiao	Update MCU decoupling, update notes, rename nets
A	22 July 2016	Jun Qiao	Update J13 setting, update power to RV1, update notes
A1	26 Aug 2016	Jun Qiao	Update FRDM+ connection compatible to DEVKIT-MOTORGF
A2	5 Sept 2016	Jun Qiao	Add test points
A3	7 Sept 2016	Jun Qiao	Change U15 to NX5P2190UKZ, change R57 to 100K
A4	9 Sept 2016	Jun Qiao	Remove D8, add J39
A5	13 Sept 2016	Jun Qiao	Set power net 12V_IN at U1 pin 1, add R88
A6	20 Sept 2016	Jun Qiao	Change R56 from 10K to 20K, and connected to P3V3_SDA
A7	23 Sept 2016	Jun Qiao	Change U15 to MIC2005-0.8YM6, remove R57, change R56 to 10K, add C87.
B	28 Sept 2016	Jun Qiao	Release

Notes:

- All components and board processes are to be ROHS compliant
- All capacitors are 10% tolerance unless otherwise stated
- All resistors are 5% tolerance unless otherwise stated
- All zero ohm links are 0603
- All connectors and headers are denoted Px and are 2.54mm pitch unless otherwise stated
- All jumpers are denoted Jx. Jumpers are 2mm pitch
- Jumper default positions are shown in the schematics. For 3 way jumpers, default is always posn 1-2
  2 Pin jumpers generally have the "source" on pin 1
- All switches are denoted SWx
- All test points (SMT wire loop style) are denoted TPx
- Test point Vias (just through hole pads) are denoted TPVx

3 Different test points used in design:

TPVx - Through Hole Pad small

TPHx - Through Hile Pad Large (for standard 0.1" header).
Also used on IO Matrix (IOMx)

TPX - Surface Mount Wire Loop

User notes are given throughtout the schematics.

Specific PCB LAYOUT notes are detailed in ITALICS

Caution:

These schematics are provided for reference purposes only. As such, NXP does not make any warranty, implied or otherwise, as to the suitability of circuit design or component selection (type or value) used in these schematics for hardware design using the NXP Calypso family of Microprocessors. Customers using any part of these schematics as a basis for hardware design, do so at their own risk and Freescale does not assume any liability for such a hardware design.

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ICAP Classification: CP: IUO: X PUBI:

Designer: Jun Qiao	Drawing Title: DEVKIT-MPC5744P		
Drawn by: Jun Qiao	Page Title: Index, Rev, Notes		
Approved: Pesses Philip	Size: C	Document Number: SCH-29333 PDF: SPF-29333	Rev: B
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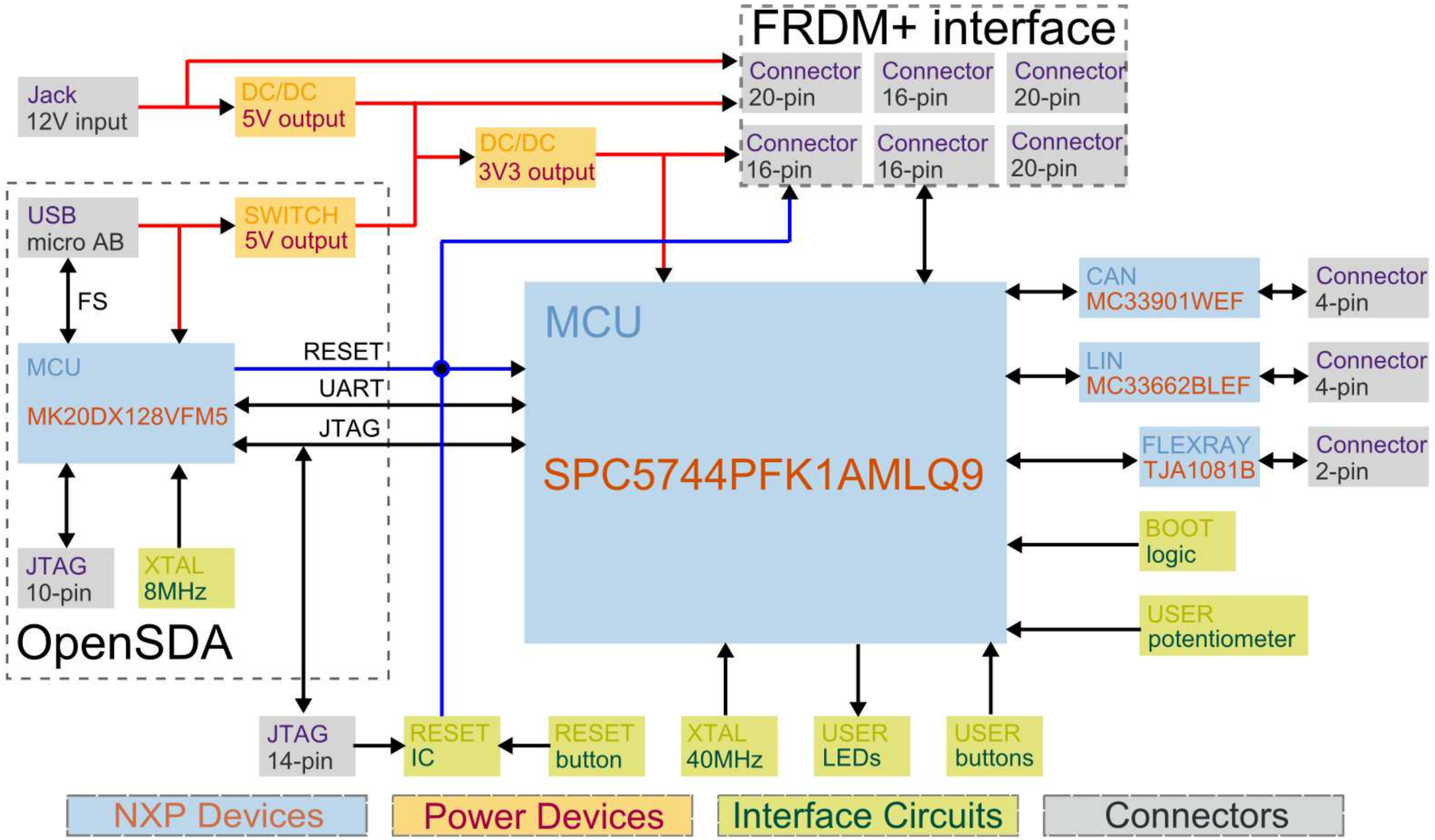
Block Diagram



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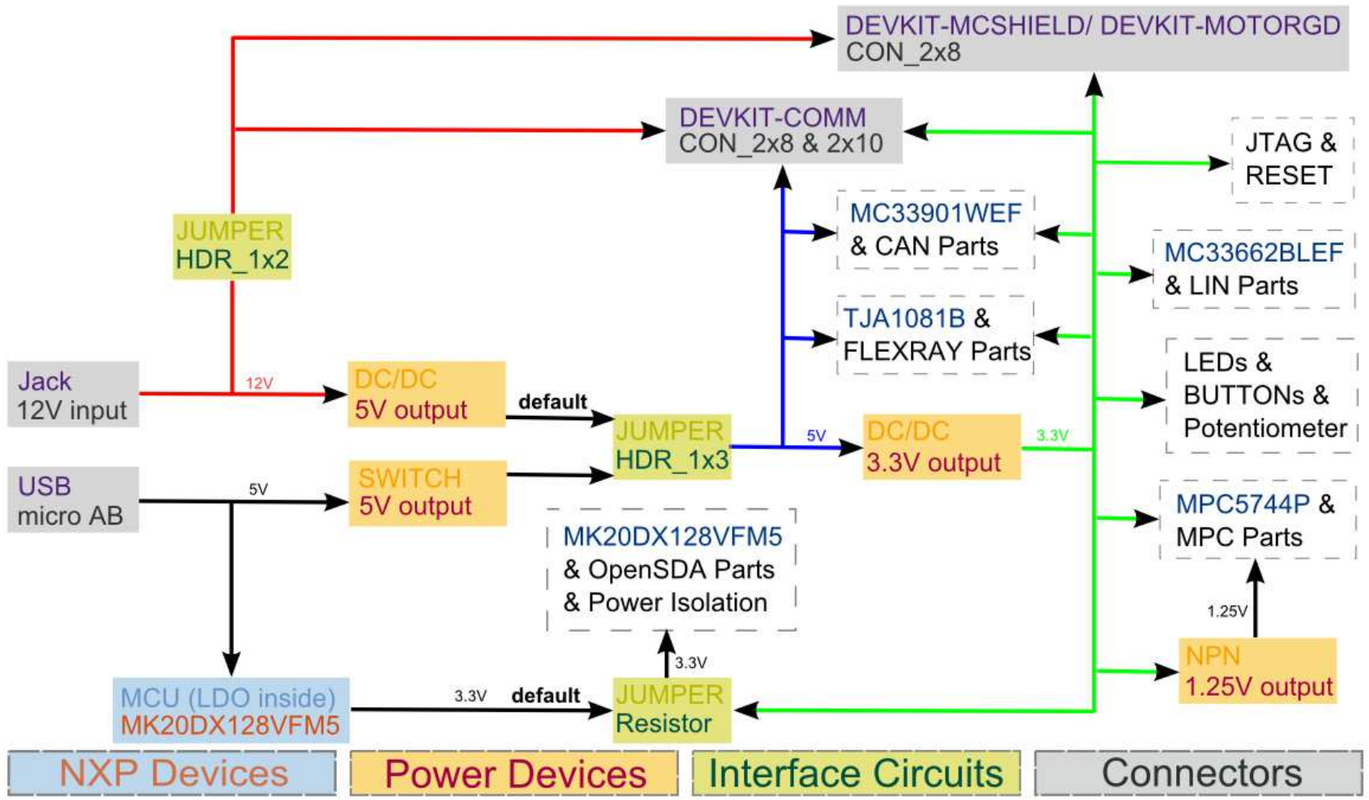
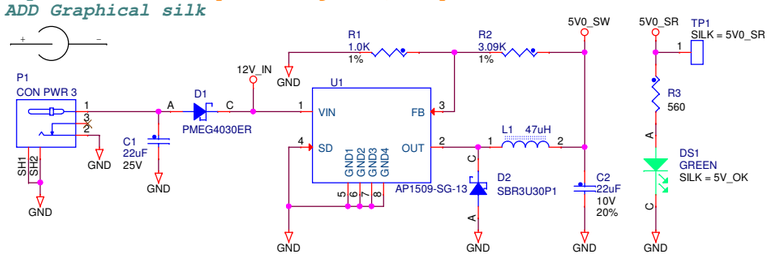
Board Power



5V Switching Regulator

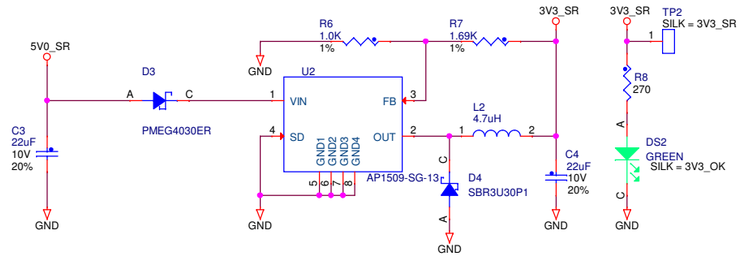
Layout note: Input Voltage 12V, Output 5V at 1800mA
ADD Graphical silk



Layout note: follow IC datasheet recommandations for PCB layout and thermal dissipation

3.3V Switching Regulator

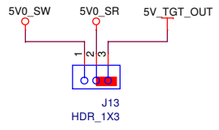
Input Voltage 5V, Output 3.3V at 1600mA



Layout note: follow IC datasheet recommandations for PCB layout and thermal dissipation

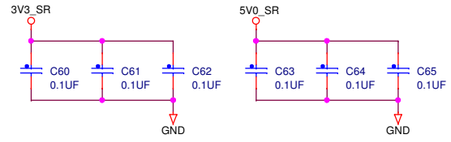
Board supply selection

Select between USB and external 12V



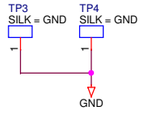
1-2 -> external 12V
2-3 -> USB/UART connector

3.3V & 5V Power Decoupling



Layout note:
Decoupling distributed uniformly

Test and reference points



Layout note:
GND Test Points, Top Side

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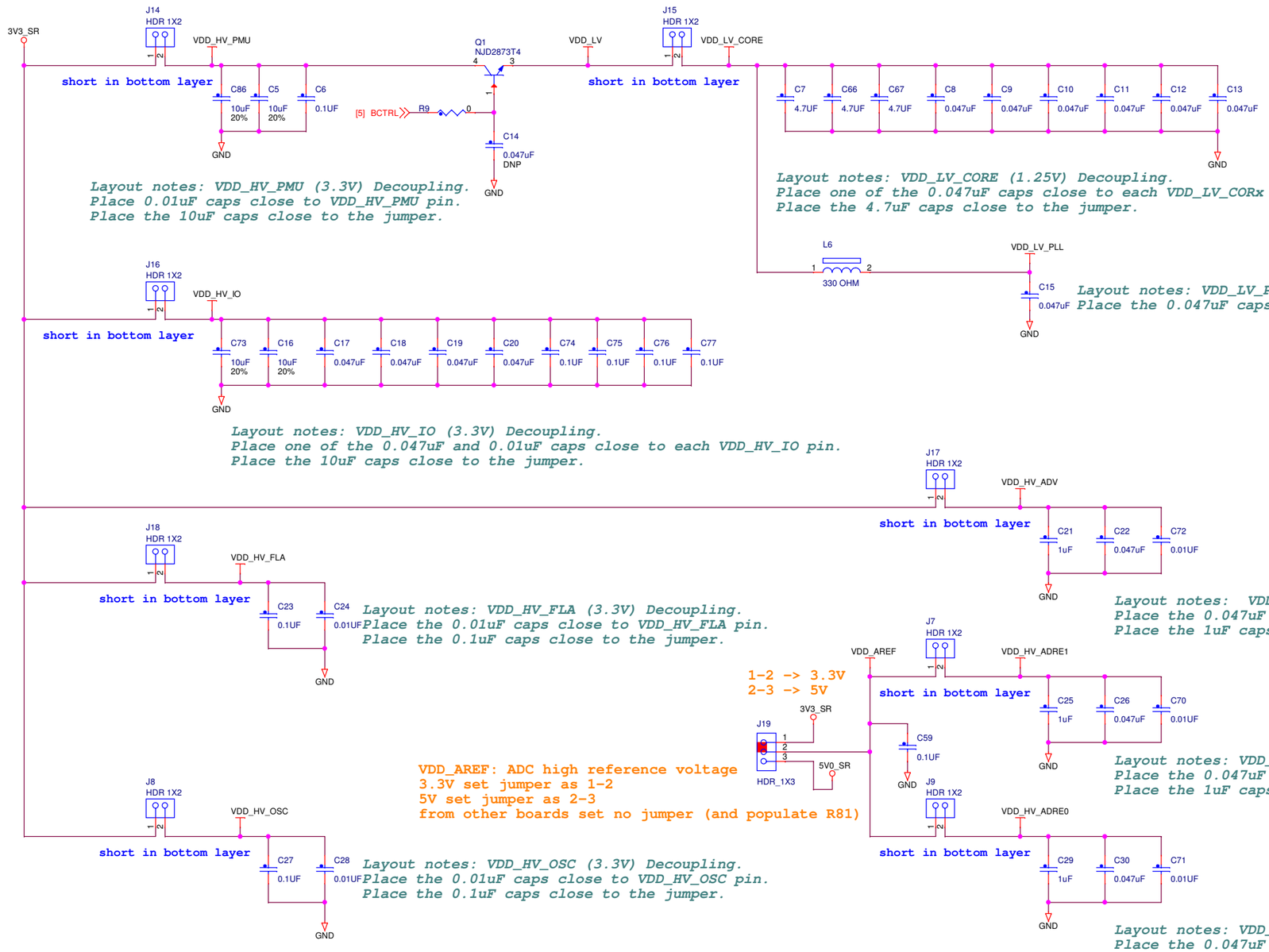
MCU Power

MCU Power Decoupling

Default Configuration:
- MCU supply voltages (VDD_HV_IO, VDD_HV_PMU, VDD_HV_OSC, VDD_HV_ADV, VDD_HV_FLA) are set to 3.3V
- MCU core voltage (VDD_LV_CORE, VDD_LV_PLL) are set to 1.25V
- MCU analog reference voltage (VDD_HV_AREx) are set 3.3V default. Could be 5V, or from external J2 pin15 (3.15V~5.5V).

VDD_HV_ADRE0 and VDD_HV_ADRE1 cannot be operated at different voltages and need to be supplied by the same voltage source.



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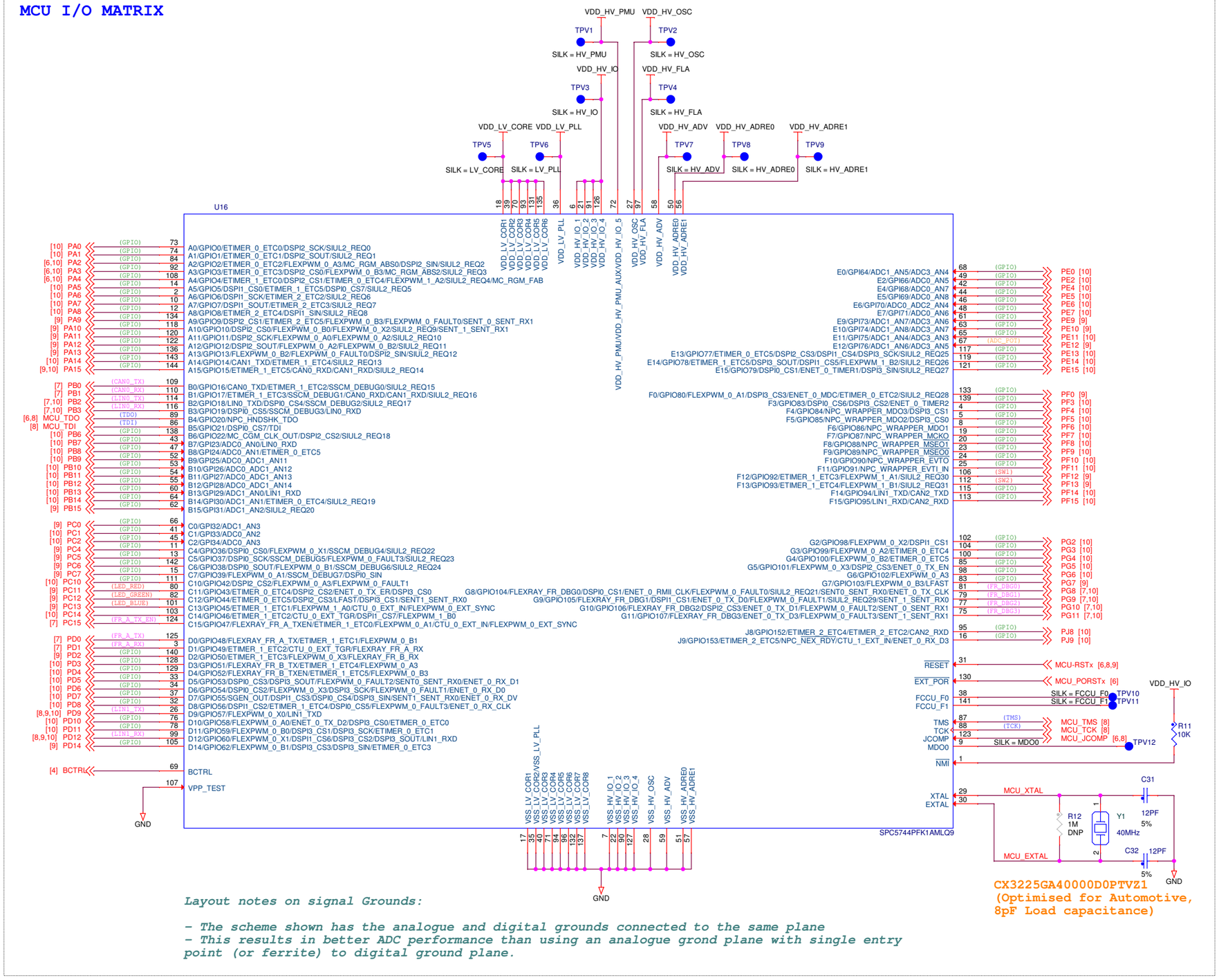
MCU Pins

MCU I/O MATRIX



Layout notes on signal Grounds:

- The scheme shown has the analogue and digital grounds connected to the same plane
- This results in better ADC performance than using an analogue grond plane with single entry point (or ferrite) to digital ground plane.

Key to text colours:

- Purple - Comms Physical Interfaces
- Orange - Other Peripherals and I/O
- Blue - Debug (JTAG & Nexus)
- Black - Clock, Reset and Control
- RED - I/O Matrix and other functions (eg. LED, BUTTON)
- Green - I/O Matrix (dedicated)

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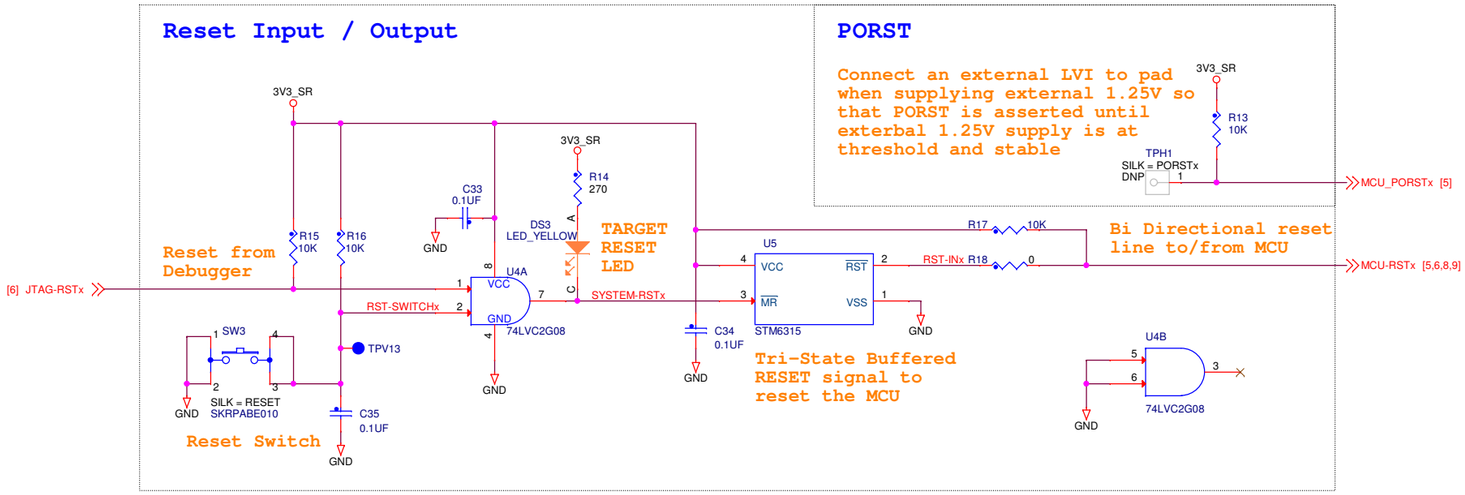
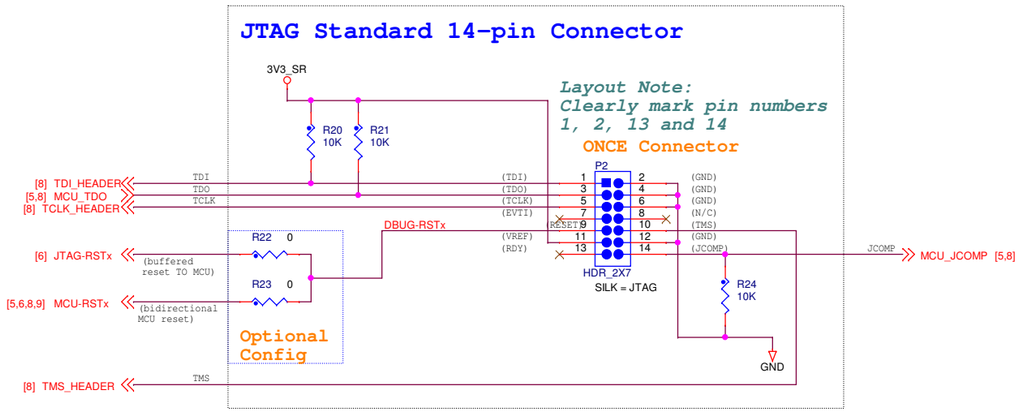
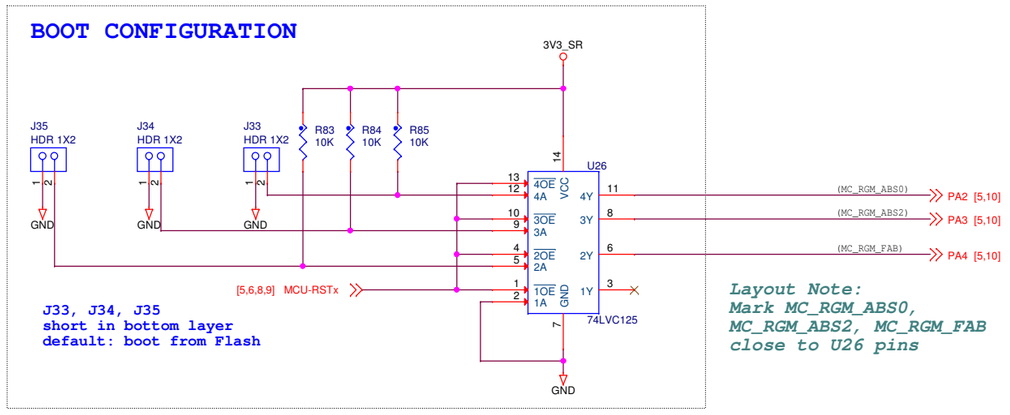
Boot, Reset & JTAG



Pin/ball startup and reset states

Pin/ball	Startup state	State during reset	State after reset
GPIOs	hi-z	hi-z	hi-z
Analog inputs	hi-z	hi-z	hi-z
JCOMP (TRST)	hi-z	input, weak pull-down	input, weak pull-down
TDI	hi-z	input, weak pull-up	input, weak pull-up
TDO	hi-z	output, hi-z	output, hi-z
TMS	hi-z	input, weak pull-up	input, weak pull-up
TCK	hi-z	input, weak pull-up	input, weak pull-up
XTAL/EXTAL	hi-z	hi-z	hi-z
FCCU_F[0]	hi-z	input, hi-z	output/input, hi-z
FCCU_F[1]	hi-z	input, hi-z	output/input, hi-z
EXT_POR_B	hi-z	input, weak pull-down	input, weak pull-down
RESET_B	hi-z	input, weak pull-down	input, weak pull-down
NMI_B	hi-z	input, weak pull-up	input,weak pull-up
FAB	hi-z	input, weak pull-down	input, weak pull-down
ABS[2]	hi-z	input, weak pull-down	input, weak pull-down
ABS[0]	hi-z	input, weak pull-down	input, weak pull-down





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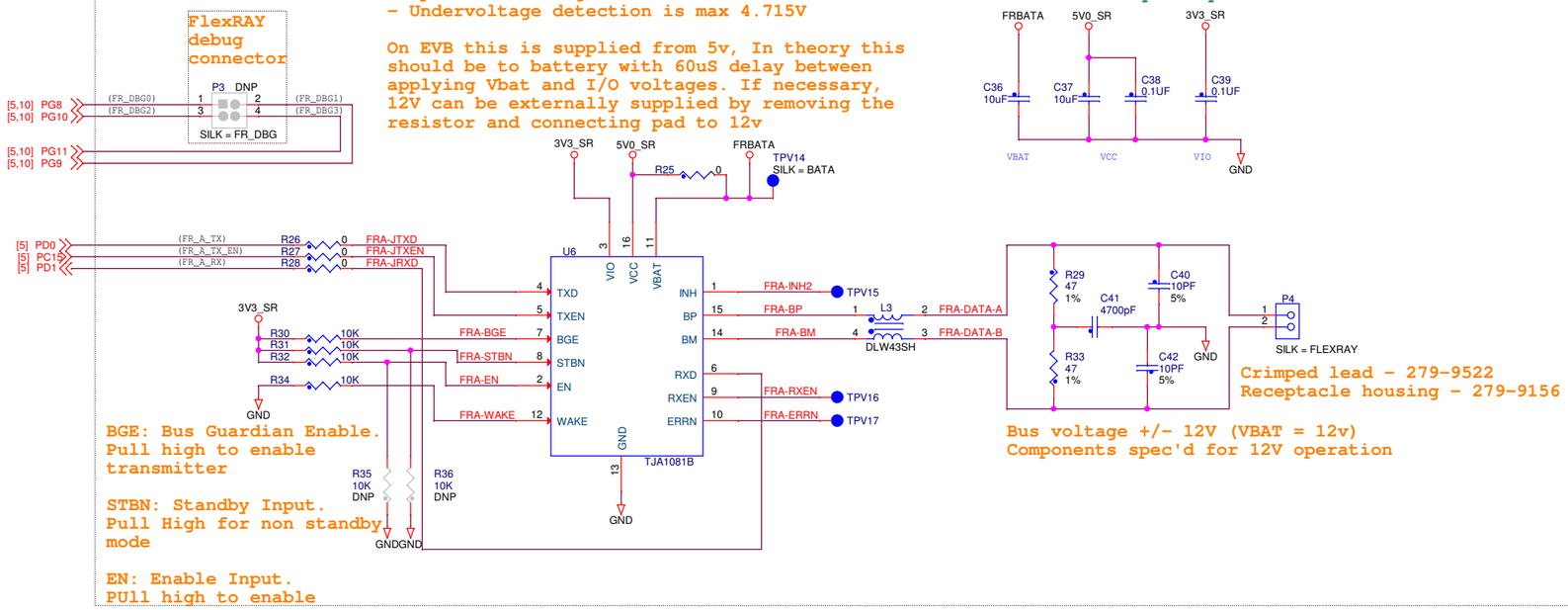
Flexray, CAN, LIN

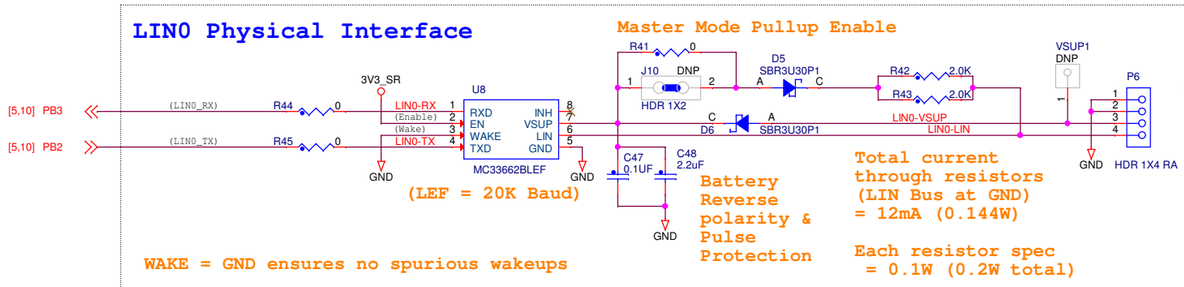
State transitions forced by EN and STBN
→ indicates the action that initiates a transaction

Transition from mode	Direction to mode	Transition number	Pin	
			STBN	EN
Normal	Receive-only	1	H	→ L
	Go-to-sleep	2	→ L	H
	Standby	3	→ L	→ L
Receive-only	Normal	4	H	→ H
	Go-to-sleep	5	→ L	→ H
	Standby	6	→ L	L
Standby	Normal	7	→ H	→ H
	Receive-only	8	→ H	L
	Go-to-sleep	9	L	→ H
Go-to-sleep	Normal	10	→ H	H
	Receive-only	11	→ H	→ L
	Standby	12	L	→ L
	Sleep	13	L	H
Sleep	Normal	14	→ H	H
	Receive-only	15	→ H	L
	Standby	16	→ H	X

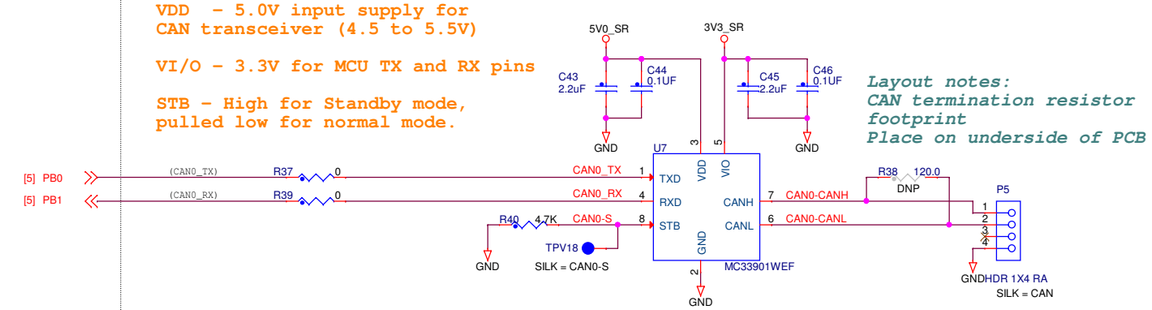
FLEXRAY_A Physical Interface



LIN0 Physical Interface



CAN0 Physical Interface



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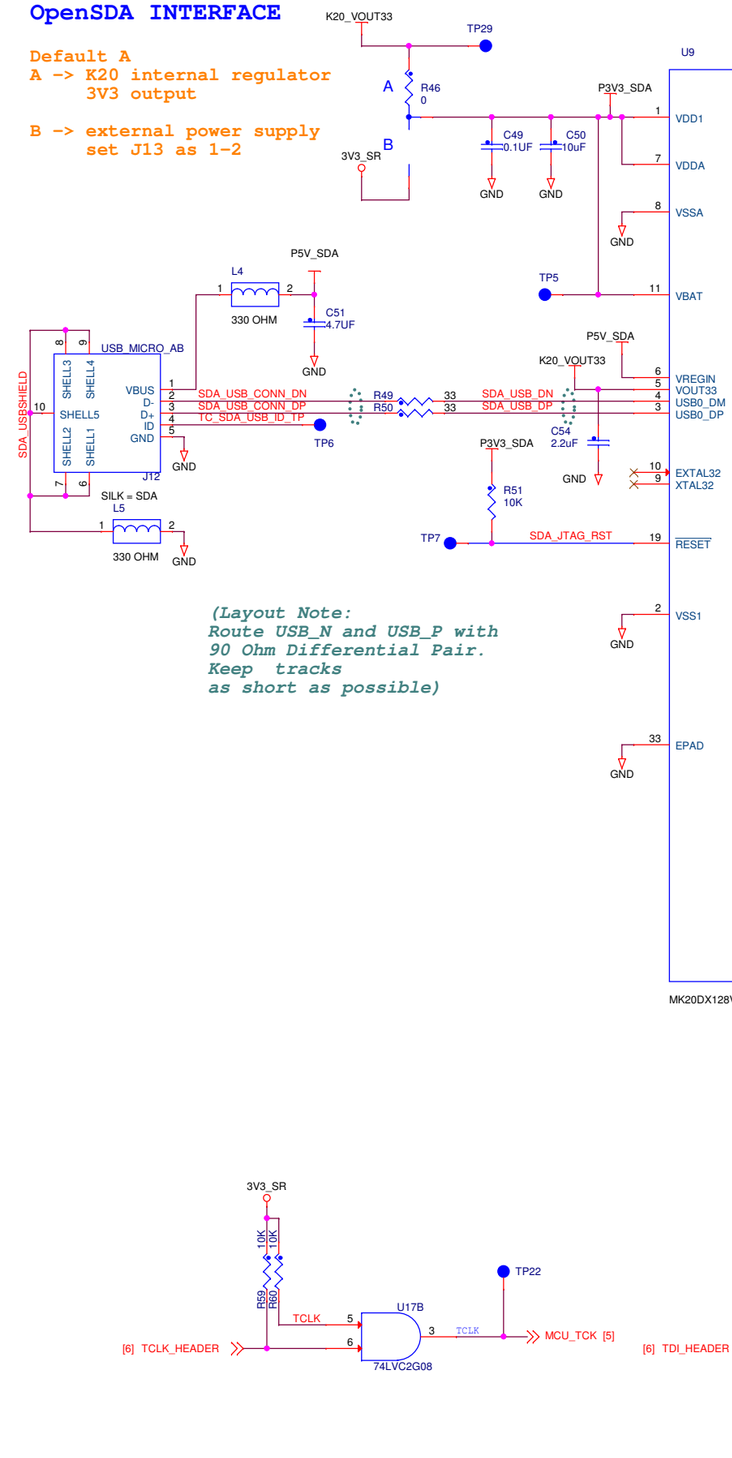
OpenSDA

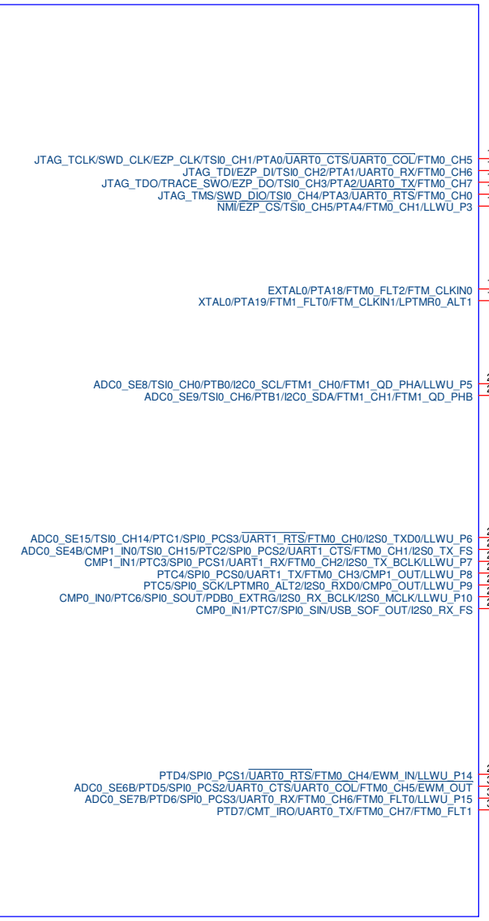
OpenSDA INTERFACE

Default A
A -> K20 internal regulator
3V3 output

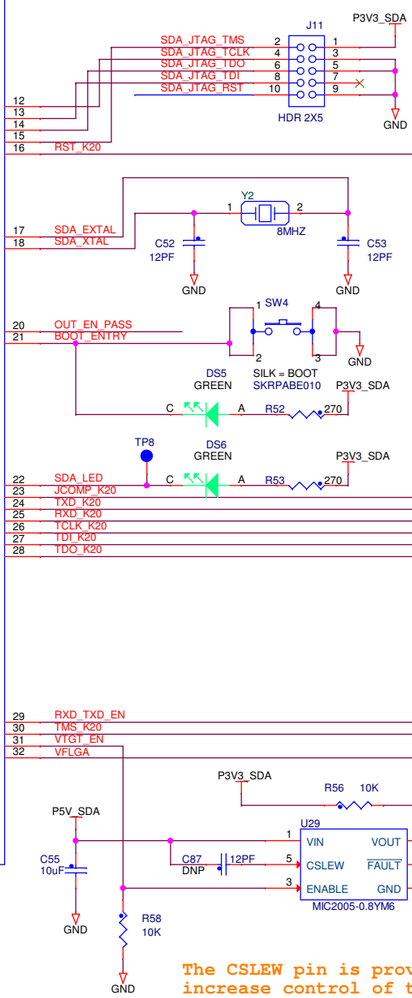
B -> external power supply
set J13 as 1-2



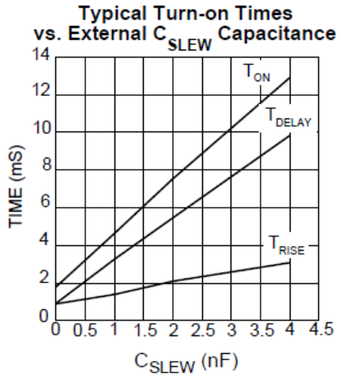
(Layout Note:
Route USB_N and USB_P with
90 Ohm Differential Pair.
Keep tracks
as short as possible)

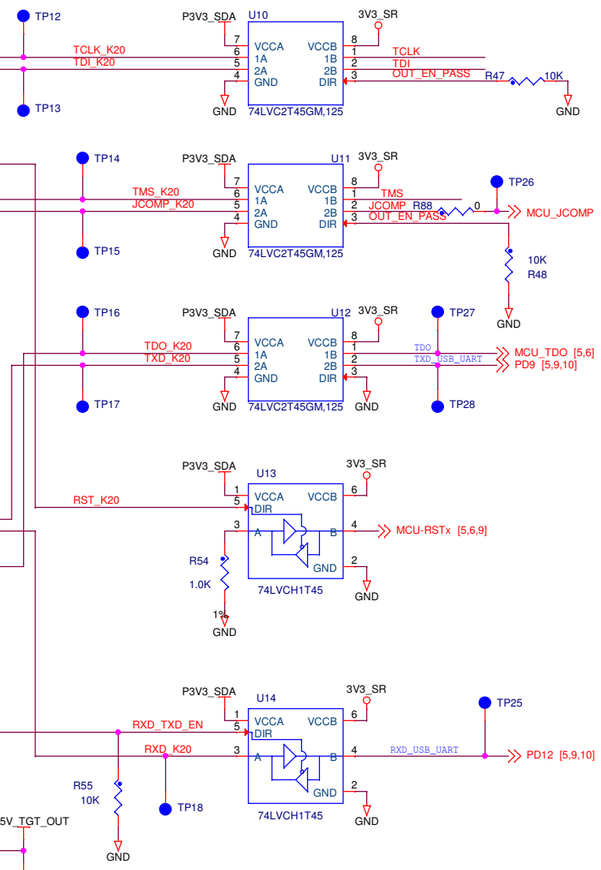


OpenSDA INTERFACE JTAG CONNECTOR



The CSLEW pin is provided to increase control of the output voltage ramp at turn-on.
The upper limit on the value of C87 is 4nF.
Herein, C87 is DNP - only a footprint for further use.





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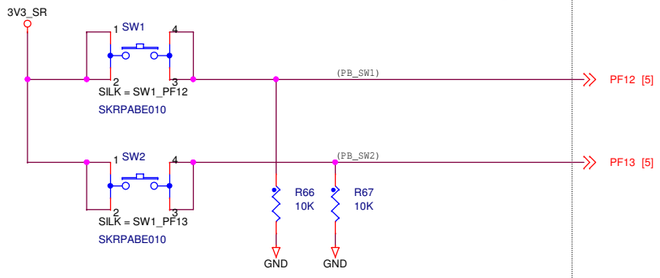
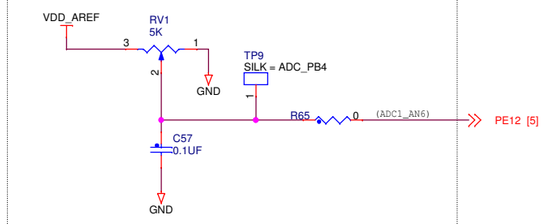
User Peripherals

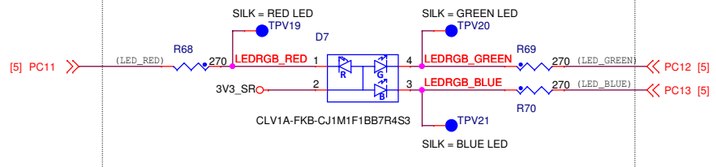
User Pushbutton Switches (Active High)



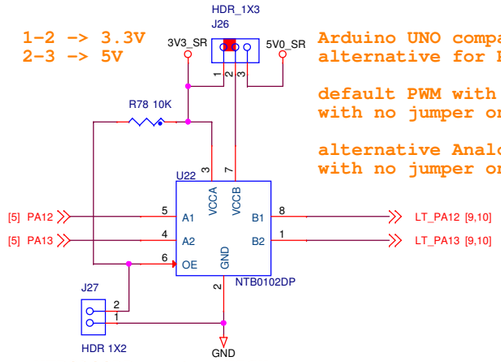
ADC Input Pot and Test Point

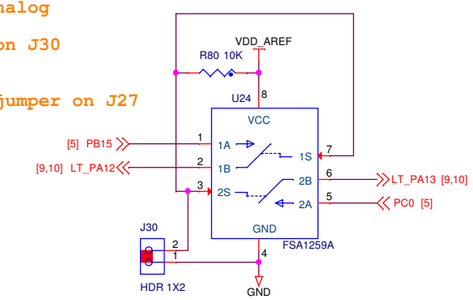


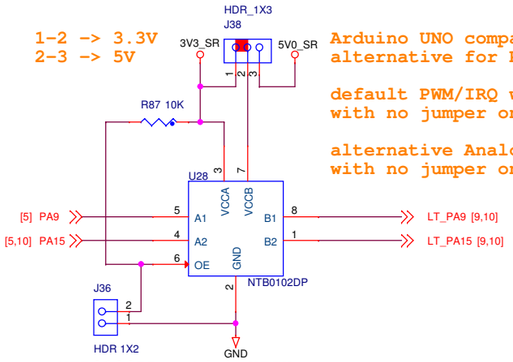
User RGB LED (Active Low)

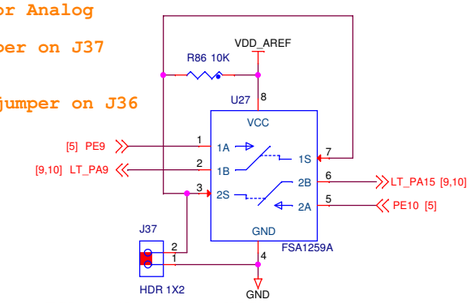


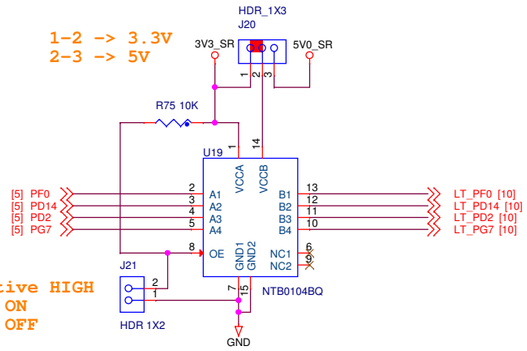
LEVEL TRANSLATOR FOR FRDM+

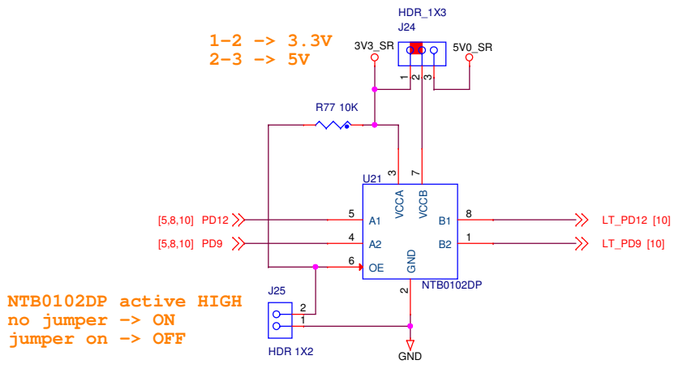


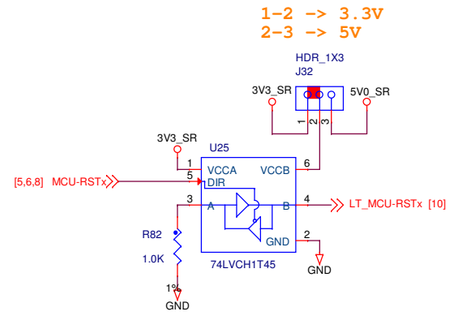


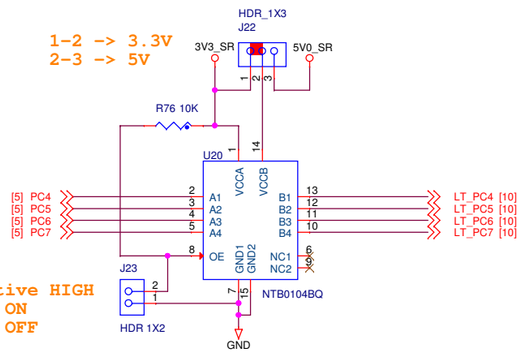


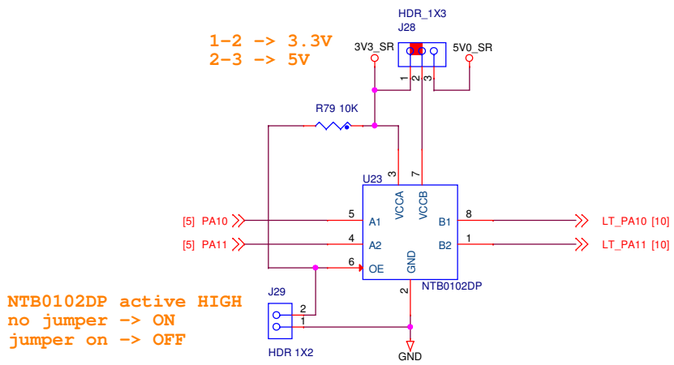












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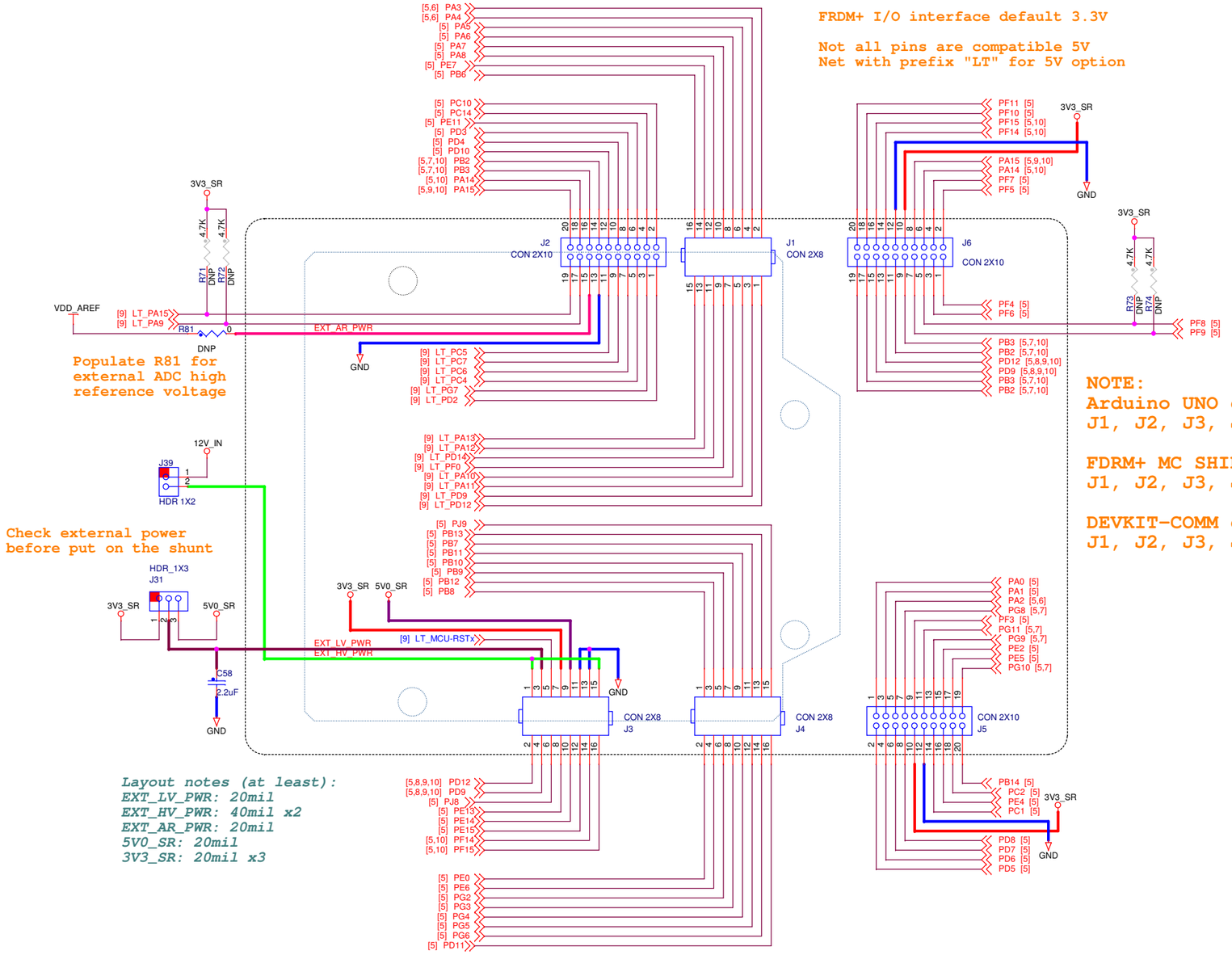
FRDM+ Connectors



NOTE:
Arduino UNO compatible headers:
J1, J2, J3, J4

FDRM+ MC SHIELD/DEVKIT-MOTORGD compatible headers:
J1, J2, J3, J4, J5

DEVKIT-COMM compatible headers:
J1, J2, J3, J4, J5, J6

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